A Direct-Conversion W-CDMA Front-End SiGe Receiver Chip

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Abstract **— A W-CDMA direct-conversion front-end receiver chip consisting of a low-noise amplifier (LNA), a dual-gain RF variable-gain amplifier (RF-VGA), two direct-down-conversion mixers, a I/Q quadrature generator, and a base-band five-gain-stage VGA is designed and manufactured in a 0.25μm IBM SiGe BiCMOS production process. A very low DC offset value (<300 μV) is measured at the output of the mixers as the LO signal is fed into the chip at twice the RF frequency. An extremely low local oscillator (LO) leakage of –105 dBm is measured at the LNA input, partly due to the excellent LO-to-RF isolation provided by the RF-VGA and the direct-conversion mixers. The measured cascaded noise figure for the chip (including the SAW filter) is 4.3 dB at the maximum gain mode, and the IIP2 and IIP3 are +37 and –16.5 dBm, respectively. The I/Q channels exhibit a small mismatch in magnitude (<0.1 dB) and in phase (1°-1.5°). The chip draws 24.9 mA from a 2.85V supply. The overall chip performance meets all the essential parameters of W-CDMA receiver front-end specs.**

I. INTRODUCTION

The third-generation Universal Mobile Telecommunication System (UMTS) is currently being standardized by the third-generation partnership project (3GPP) forum [1]. Using the Wide-Band Code Division Multiple Access (W-CDMA) technology for the radio interface in Japan and Europe, data rates of up to 2 Mbits/s can be delivered for in-door stationary users and up to 384 kbit/s for wide-area mobile users [2]. Recent revisions to the standardization document on the W-CDMA proposal made it possible to predict the required radio-frequency (RF) front-end performance [3]. Since in the UMTS system the signal bandwidth is adjustable, the direct-conversion (i.e., homodyne) receiver architecture is particularly suitable for UMTS implementation where the bandwidth of the receiver is determined by the cut-off frequency of the low-pass filters in the baseband. The direct-conversion receiver architecture is also preferred for cell phone applications since it can provide very high integration, lower current consumption, and lower costs by reducing the off-chip components [4]. However, it is well-known that the direct-conversion receiver suffers from DC offsets generated from LO leakage, self-mixing, finite intercept-point of second-order (IIP2), etc. [4,5]. There have been several recent reports that demonstrated the feasibility of W-CDMA direct-conversion receivers [6-9]. Since the RF signal for W-CDMA receivers consists of several code channels of high crest factors that has strong variations in the signal envelope, it can then be demodulated by the even-order non-linearity and creates IM2 distortion [3]. Besides the issue of DC offsets, it is challenging to meet the overall receiver sensitivity, selectivity, and dynamic range as the overall Noise Figure needs to be ≤9 dB (including the 3.5-4dB loss from the switch and the diplexer), and the IIP3 needs to be high enough to pass the intermodulation/blocker tests while consuming the lowest DC power possible. The strong signal leakage from the transmitter through the diplexer can also interact with the LO signals leaked from the mixers to generate DC offsets.

When designing the W-CDMA direct-conversion receiver, it is therefore of paramount importance to minimize the DC offsets induced by the LO signal and/or the RF signals/blockers/interferers. This can only be possible by achieving exceptional low LO leakage and a very high IIP2 value for the receiver front-end. In this paper, we report a W-CDMA direct-conversion front-end IC that has a measured LO leakage of –105dBm and with less than 300 μV LO-induced DC offset at the mixers output. To the best of our knowledge, the reported LO leakage and the DC offset values are the best in the literature for W-CDMA direct-conversion receiver chip. The chip is fabricated in the 50/65 GHz f_t/f_{max} SiGe 0.25μm BiCMOS production process of IBM Microelectronics. This process includes 6 levels of metal with a 4μm top metal layer, offering high-Q passives such as scalable inductors and MIM capacitors.

II. DESCRIPTION ON W-CDMA DIRECT CONVERSION IC

The direct-conversion receiver front-end IC contains a LNA, a dual-gain RF-VGA, two direct-down-conversion

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mixers, and a base-band five-gain-stage VGA. The IC also includes a quadrature generator which provides the LO inputs to the I/Q channels of the mixers from an off-chip source at twice the RF frequency. Figure 1 shows a functional block diagram of the IC. The only off-chip elements required for the front-end receiver IC are a single-ended-to-differential surface-acoustic-wave (SAW) filter, an off-chip load inductor and a bias-setting resistor for the LNA. Control circuitry provides the ability to set the chip to various gain settings and power ON/OFF modes. Note that since the strong LO signal can leak to the RF port of the mixer by capacitive, substrate and/or bond wire coupling, we decided to feed the LO signal into the front-end IC at twice the RF frequency, removing the bond-wire coupling path to lower the LO leakage.

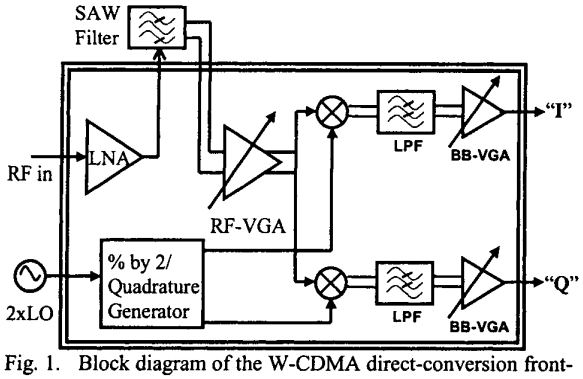

Fig. 1. Block diagram of the W-CDMA direct-conversion front-end receiver chip.

Fig. 2 shows a schematic of the LNA, which uses a common-emitter configuration with inductor degeneration to achieve good linearity. No input matching element is required for this design. For the current version of the chip, the load inductor is placed off-chip and the bias is also set by an off-chip precision resistor.

The RF signal is amplifed by the LNA and goes off-chip through the SAW filter that has a differential output. The primary functions of this RF-VGA block are: (1) the high-gain (HG) mode to amplify the weak in-band RF signals to increase the receiver sensitivity; (2) the low-gain (LG) mode to attenuate the impacts of large RF signals (including blockers and TX leakage) to mitigate the mixer IIP3 and IIP2 design requirement; (3) to increase the reverse-isolation for improving the LO leakage; (4) to perform impedance transformation required for the SAW filter output to the mixers input. One salient feature of this RF-VGA implementation is in its low power consumption with high linearity, especially for the LG mode. It also incorporates all matching elements on-chip. Fig. 3 shows the block diagram of the RF-VGA and its connections to the mixers. Note the RF outputs are AC coupled to the I/Q mixers so that the low frequency distortion generated by the 2nd order non-linearities in the LNA is blocked to prevent leakage through the mixers to the BB-VGA.

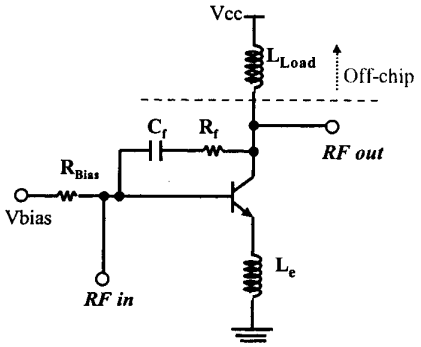

Fig. 2 Schematic of the low noise amplifier (LNA)

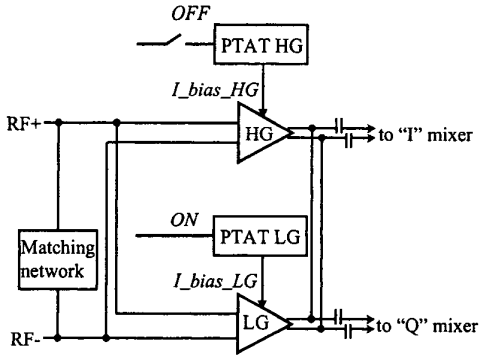

Fig. 3. Block diagram showing how the dual-gain RF-VGA is implemented (low-gain mode selected).

The I/Q direct-conversion mixers are double-balanced Gilbert-type mixer topology as shown in Fig. 4. This topology is well-understood as it provides high LO-to-RF isolation, excellent IIP2, and low DC offsets [3]. Since the 1/f noise spectrum of the mixers falls in the same band as the down-converted signals, only SiGe HBTs were used in the mixers design to minimize the 1/f noise. A low-pass filter is also placed at the output of the mixers (not drawn) before the BB-VGA to reduce the linearity requirements imposed on baseband amplifers by the blockers and adjacent channel interference (ACI) [6].

The I/Q quadrature generation is done by a master-slave toggle flip-flop. Fig. 4 shows the block diagram of the quadrature generator. The BB-VGA consists of five gain stages that offers voltage gain in 4dB step (i.e., 0,4,8,12, and 16 dB). Its main purpose is to boost the down-converted signals to mitigate noise problems in transferring signals from the receiver front-end IC to an analog-base-band (ABB) chip. All circuits are simulated

for power supply, temperature, and process variations with parasitic extraction tools. Every single I/O pin of the IC is protected by ESD diodes, including the RF input pins.

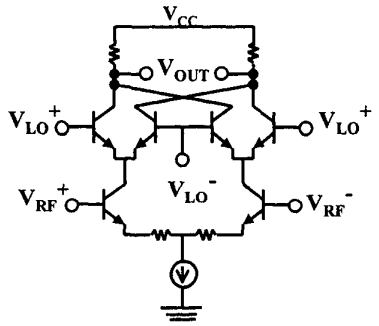

Fig. 4 Schematic of the down-conversion double-balanced mixer.

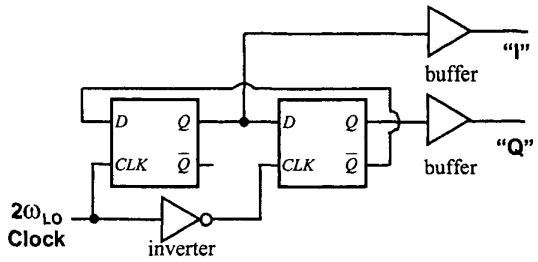

Fig. 5 A block diagram showing the I-Q quadrature generator.

III. MEASUREMENT RESULTS

Fig. 6 shows the measured LNA performance. The simulated S-parameters and Noise Figure using Cadence SpectreRF are in close agreement with the measured data, suggesting the accuracy in the modeling of active devices, the inductors, and the parasitics. Table (I) lists the measured circuit performance for each block, which are again rather close to the simulated values. For example, the gain step and the P1dB points of the RF-VGA are both within 1dB from the simulated data. The LNA has high linearity and low Noise Figure (NF=1.6dB), and the mixer has excellent LO-to-RF isolation of 69.5 dB. The I/Q mismatches are low in both magnitude and in phase.

Fig. 7 plots the measured LO leakage at the input of the LNA vs. the LO power. A LO signal power of –13 dBm at 4280 MHz was applied to the board and the signal power at the LNA input at 2140 MHz was measured. One can see that the LO leakage is not sensitive to the LO signal power and it is below –103 dBm. This excellent LO leakage is achieved partly because the LO signal is fed to the chip at 2xRF frequency so the leakage path at the RF frequency through the bond wires is eliminated. However, we also believe that the architecture selection of placing a dual-gain RF-VGA in front of the mixers is the key reason in obtaining this extremely low LO leakage, as the dual-gain RF-VGA provides >30 dB reverse isolation. Since the measured LO-to-RF isolation from the mixer is close to 70 dB and the LNA provides an additional 20 dB reverse isolation, the LO leakage at the input of the LNA can be as low as –120 dBm. However, the substrate coupling is likely to have limited this isolation to –105 dBm.

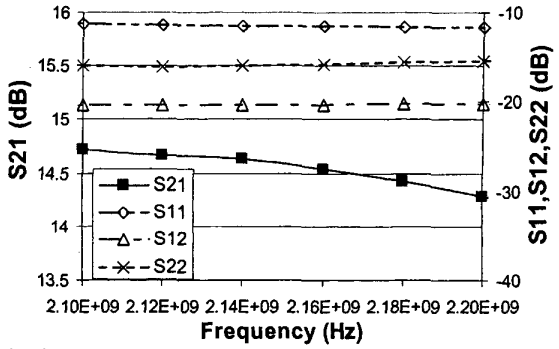

Fig. 6. Measured S-parameter performance for the LNA.

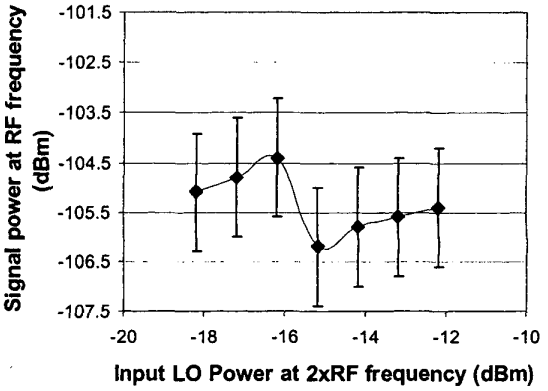

Fig. 7. Measured LO leakage of the front-end receiver IC.

Fig. 8 shows a picture of the RF evaluation board that features the front-end receiver IC in a QFN32 package. The chip is bonded on a high-frequency Teflon printed circuit board that is compatible with the standard FR4. Table (II) shows the key measured performance table for the W-CDMA front-end receiver chip. Several samples have been measured and by two different sites to ensure proper data reliability. The IIP3 was measured at LO=4.28GHz with two tones at offset frequencies of 10 and 19 MHz (each of –50 dBm). Extremely low LO-induced DC offsets are found at the mixers output (<300 μV) and at the BB-VGA output (<2mV). The overall chip performance meets all the essential parameters of W-CDMA receiver front-end specs [3].

Table (I) Measured performance table for each circuit block

Blocks Performance	Measured	unit
LNA Gain	14.5	dB
LNA NF	1.6	dB
LNA IIP3	5	dBm
LNA Idc	8.7	mA
LNA Isolation	20	dB
LNA Input Match (S11)	<-11	dB
LNA Output Match (S22)	<-14	dB
RF-VGA Gain Step	21+/-1	dB
RF-VGA HG P1dB	-11.5	dBm
RF-VGA HG Idc	2.6	mA
RF-VGA LG P1dB	> +3.5	dBm
RF-VGA LG Idc	2.4	mA
Mixer P1dB	>-11.4	dBm
Mixer IIP3	>-4	dBm
Mixer LO-to-RF isolation	69.5	dB
Mixer Voltage Gain	>0	dB
Mixer IIP2	>38	dBm
Mixer Idc	3.3	mA
I/Q Channel Phase Error	1-1.5	degree
I/Q Channel Magnitude Error	0.09	dB
Quad Generator Idc	3.8	mA
BB-VGA Gain Step (5 steps)	4+/-0.15	dB
BB-VGA Idc	3.2	mA

Table (II) Measured key performance table for the entire RF chip

Cascaded IC Performance (with SAW)	Measured	unit
Cascaded max. Voltage Gain	45.7	dB
Cascaded min. Voltage Gain	8.7	dB
LO Leakage (in front of LNA)	-105 +/-2	dBm
Cascaded IIP2 (max. gain; in-band signals)	36.6	dBm
Cascaded IIP3 (max. gain; in-band signals)	-16.5	dBm
P1dB (max. gain but no BBVGA, in-band)	-26.3	dBm
Cascaded DSB Noise Figure (max. gain)	4.3	dB
LO Induced DC Offset @Mixer output	<0.3	mV
LO Induced DC Offset @BBVGA output	<1.9	mV
Total Idc (entire chip)	24.9	mA
Idc RF blocks only (LNA+RF-VGA+Mixers)	17.9	mA
Power Supply Voltage	2.85	V
S11	<-11	dB
Total Gain Control Range	37	dB
Chip Area	2.25x2.6	mm^2

IV. CONCLUSION

A W-CDMA direct-conversion front-end receiver chip implemented in a 0.25μm SiGe BiCMOS production process is reported. An extremely low LO leakage of –105 dBm is measured at the LNA input. A very low DC offset value (<300μV) is induced by the LO signal at the output of the mixers. The 37dB gain control range provides increased linearity for high input signal levels. The measured cascaded Noise Figure for the chip (including the SAW filter) is 4.3 dB at the maximum gain mode. The overall chip performance meets all the essential parameters of W-CDMA receiver front-end specs under nominal operating condition.

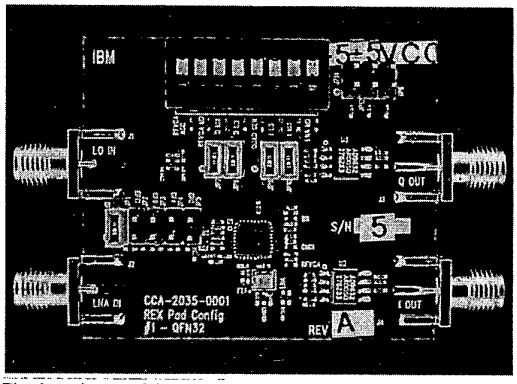

Fig. 8 A picture of the evaluation board with the packaged receiver chip.

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